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CLAIM AMENDMENTS

Claims 1-15 are pending. Claim 1 has been currently amended.

1. (Currently Amended) A video signal processing integrated circuit for use in a video recording/reproducing apparatus, the video signal processing integrated circuit comprising, as a single chip:

a video recording/reproducing processor for providing a video signal to be recorded on a storage medium and for reproducing a video signal recorded on said storage medium;

a composite synchronization dividing unit for separating a composite synchronization signal from a video signal output by said video recording/reproducing processor;

a vertical synchronization dividing unit for separating a vertical synchronization signal from the composite synchronization signal;

a quasi vertical synchronization inserting unit for inserting a quasi vertical synchronization signal in the video signal output from said video recording/reproducing processor;

a single pin port for outputting the vertical synchronization signal from said video signal processing integrated circuit and inputting a quasi vertical synchronization signal to said video signal processing integrated circuit, said single pin port to operate as an input port for inputting said quasi vertical synchronization signal in a special reproducing mode, and to operate as an output port for outputting the vertical synchronization signal in all other modes of said video signal processing integrated circuit; and

a switching unit for providing the vertical synchronization signal, which is input from the

vertical synchronization dividing unit, to the pin port, or providing the quasi vertical synchronization signal, which is input from the pin port, to the quasi vertical synchronization inserting unit.

2. (Original) The video signal processing integrated circuit of claim 1, wherein the pin port is designed to operate as an input port in a special reproducing mode, and operate as an output port in a recording mode or a normal reproducing mode.

3. (Original) The video signal processing integrated circuit of claim 1, wherein the switching unit controls connections so that in a special reproducing mode, a quasi vertical synchronization signal, which is input to the pin port, is output to the quasi vertical synchronization inserting unit, and all other modes, a vertical synchronization signal output from the vertical synchronization dividing unit is output to the pin port.

4. (Original) The video signal processing integrated circuit of claim 1, further comprising another switching unit for selectively outputting from said video signal processing integrated circuit, the video signal output from said video recording/reproducing processor or the video signal output from said quasi vertical synchronization inserting unit.

5. (Original) The video signal processing integrated circuit of claim 4, wherein said another switching unit outputs the video signal output from said quasi vertical synchronization inserting unit in a special reproducing mode, and in all other modes, outputs the video signal output from said

video recording/reproducing processor.

6. (Original) A video signal processing apparatus integrated on a single chip, comprising:

a recording and reproducing processor for modulating an input video signal to be recorded on a recording medium and for demodulating a video signal reproduced from said recording medium;

a composite synchronization dividing unit for separating a composite synchronization signal from video signals output from the recording and reproducing processor;

a vertical synchronization dividing unit for separating a vertical synchronization signal from the composite synchronization signal;

a single pin port for outputting the vertical synchronization signal and inputting a quasi vertical synchronization signal;

a quasi vertical synchronization inserting unit for inserting a quasi vertical synchronization signal into a reproduced video signal output from said recording and reproducing processor;

a first switching unit for selectively providing the vertical synchronization signal from the vertical synchronization dividing unit to the pin port, or for providing the quasi vertical synchronization signal to said quasi vertical synchronization inserting unit; and

a second switching unit for selectively connecting the reproduced video signal having the inserted quasi vertical synchronization signal, output from an output terminal of the quasi vertical synchronization inserting unit, to a video output port in a special reproducing mode, and connecting the reproduced video signal, output from the recording and reproducing processor, to the video

output port in all other modes of said video signal processing apparatus.

7. (Original) The video signal processing apparatus of claim 6, wherein the pin port is designed to operate as an input port in said special reproducing mode, and to operate as an output port in a recording mode.

8. (Original) The video signal processing apparatus of claim 6, wherein the first switching unit controls connections so that the quasi vertical synchronization signal, which is input to the pin port, is output to the quasi vertical synchronization inserting unit in the special reproducing mode, and in all the other modes, the vertical synchronization signal, which is output from the vertical synchronization dividing unit, is output to the pin port.

9. (Original) The video signal processing apparatus of claim 6, having a structure wherein the pin port is connected to both a vertical synchronization signal input port and a quasi synchronization signal output port of a microprocessor.

10. (Original) The video signal processing apparatus of claim 9, wherein the vertical synchronization signal input port is in a high impedance state in a special reproducing mode, and the quasi vertical synchronization signal output port operates as an output port in said special reproducing mode and is in a high impedance state in a recording mode.

11. (Original) The video signal processing apparatus of claim 6, having a structure wherein the pin port is connected to both a vertical synchronization signal input port of a microprocessor via a first resistor and a quasi synchronization signal output port of said microprocessor via a second resistor.

12. (Original) The video signal processing apparatus of claim 11, wherein said first and second resistors are impedance matching resistors.

13. (Original) The video signal processing apparatus of claim 12, wherein the vertical synchronization signal input port is in a high impedance state in a special reproducing mode, and the quasi vertical synchronization signal output port operates as an output port in said special reproducing mode and is in a high impedance state in a recording mode.

14. (Original) A method for designing a video signal processing integrated circuit having a recording and reproducing processor for modulating/demodulating a video signal, a vertical synchronization dividing unit, and a quasi vertical synchronization inserting unit, the method comprising the steps of:

forming a single pin port for outputting a vertical synchronization signal separated from a composite synchronous signal by said a vertical synchronization dividing unit and for inputting to said video signal processing integrated circuit a quasi vertical synchronization signal produced by a microprocessor; and

designing the pin port to operate as an input port for inputting said quasi vertical synchronization signal in a special reproducing mode, and to operate as an output port for outputting the vertical synchronization signal to the microprocessor in all other modes of said video signal processing integrated circuit.

15. (Original) The method of claim 14, further comprising the step of:

selectively connecting, via a switching circuit, the single pin port and said quasi vertical synchronization inserting unit to provide said quasi vertical synchronization signal to said quasi vertical synchronization inserting unit in said special reproducing mode or connecting the single pin port to said vertical synchronization dividing unit to provide the vertical synchronization signal output from the vertical synchronization dividing unit to said single pin port in all the other modes.